ABSTRACT OF THE DISCLOSURE

Internal read out data bits are divided into a plurality of data groups, and data bits in corresponding positions in different data groups are paired off. A determination gate is provided to each pair of data bits, and determining operation is performed in each pair to compress the result of determination to finally generate a 1-bit flag indicating a match/mismatch in logic level among the internal read out data. Consequently, a multi-bit test circuit that has a reduced layout area and can perform high-speed multi-bit determination is provided.